UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
- P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,589	03/30/2004	Susanne A. Paul	SIL.P0078	4323

30163 7590 03/22/2007

JOHNSON & ASSOCIATES
PO BOX 90698
AUSTIN, TX 78709-0698

EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	**PAPER NUMBER**
2815	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/813,589	PAUL ET AL.	
	Examiner	Art Unit	
	Michael B. Shingleton	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47-62* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09-28-2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The terminal disclaimer filed 4-7-2006 has been approved.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 47-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koinuma US4,451,802 (Koinuma) in view of King US 6,300,827 (King), Engbretson US5,311,150 (Engbretson), Dudley et al. US5,144,133 (Dudley) and Mandelman et al. US6,311,531 (Mand).

FIG. 3

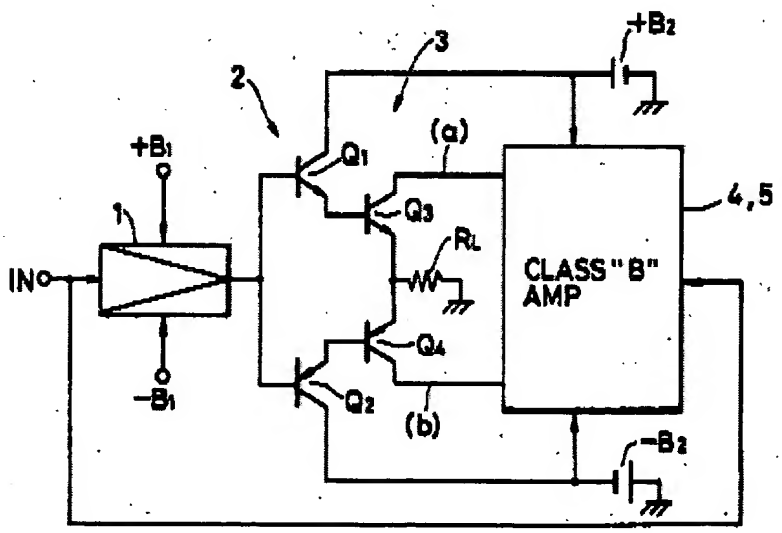


Figure 3 and the relevant text of Koinuma disclose a power amplifier arrangement and method of providing an amplifier with a preamplifier 1 (input stage) and an output stage (2 and 3) that is supplied with two different power sources (B_1 and B_2). The voltage B_2 is of a greater magnitude than that of B_1. (See column 3, around line 36)

> Since the power supplies $\pm B_2$ for the class B amplifier circuits are greater in level and in capacity than the power supplies $\pm B_1$ of the voltage amplifying stage 1 of the class A amplifier circuit,

Column 3, around line 36 of Koinuma.

Koinuma also discloses in column 1, around line 9 that the amplifiers are such that they can be classes such as class A, B and are used for powering a loudspeaker or "otherloads" (sic).

> Amplifiers for delivering output power to loudspeakers or otherloads include class A and class B power amplifier circuits.

Column 1, around line 9 of Koinuma.

Koinuma is silent on exactly what the other loads are specifically, but never the less Koinuma teaches that the invention applies to other loads as well.

One well known "other load" for a class A, B etc. amplifier is for the wireless transmission system, i.e. a cellular telephone that includes a transceiver and an antenna as evidenced by King (See the abstract and column 7, around line 21.)

> (57) **ABSTRACT**
>
> A cascaded amplifier is integrated within an integrated circuit with a cascaded ground bus. The cascaded ground bus provides two ground points at opposite ends. Each amplifier ground of each amplifier stage couples to the ground wire there between. The cascaded ground bus substantially reduces the parasitic inductance in the emitter leg of each IC transistor within each amplifier. The lay out of the cascaded ground bus wire is tightly coupled to the lay out of the input wires so that their respective parasitic inductances are magnetically coupled together to form a mutual inductance. The mutual inductance effectively cancels the effect of the ground return inductance due to them being similar inductance values and having the same ground loop current flowing through them in opposite directions. The cascaded ground bus can be utilized in substantially all amplifier types including class A, B, C, D, BD, E, F, G, H, S and their variations and with substantially all transistor types used within amplifier stages including bipolar junction transistors, field effect transistors and their variants (i.e. PNP, NPN, MOSFET, NFET, PFET, JFET, MESFET, etc.). An IC cascaded amplifier with the cascaded ground bus can be utilized in a number of communication systems where amplification is needed including battery operated systems such as a transceiver of a portable cellular telephone.

The cascaded ground bus can be utilized in substantially all amplifier types including class A, B, C, D, BD, E, F, G, H, S and their variations and with substantially all transistor types used within amplifier stages including bipolar junction transistors, field effect transistors and their variants (i.e. PNP, NPN, MOSFET, NFET, PFET, JFET, MESFET, etc.). An IC cascaded amplifier with the cascaded ground bus can be utilized in a number of communication systems where amplification is needed including battery operated systems such as a transceiver of a portable cellular telephone.

Column 7, around line 21 of King.

King is very clear that the amplifier class to be used in Cellular arrangements is that of class A, B, C, etc.. Cellular arrangements clearly have an antenna that is necessary for transmission and reception (receiving). Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the "other load" of Koinuma with a wireless transmission/reception system because as the Koinuma reference is silent on the exact structure of the "other load" one of ordinary skill in the art would have been motivated to use any art-recognized equivalent load such as the cellular antenna with transceiver as taught by King. Note that by using the arrangement of Koinuma to power an antenna that this makes the power amplifier an "RF power amplifier".

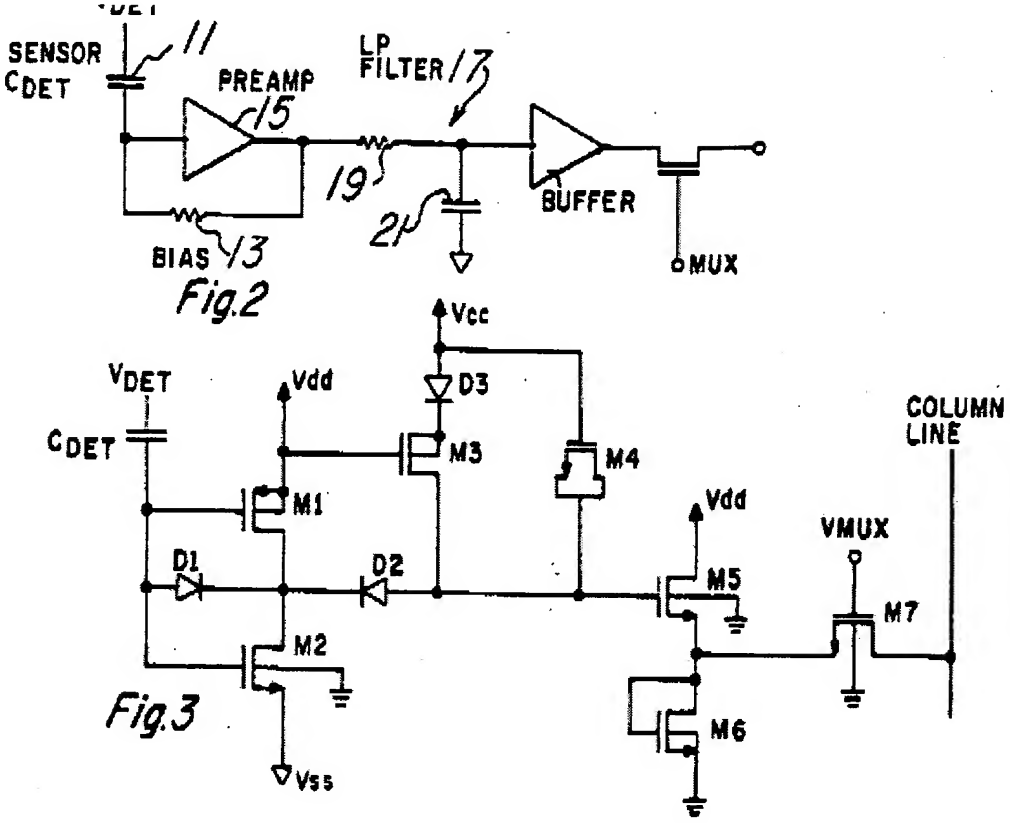
In addition to that above Koinuma is silent on the use of a CMOS based preamplifier and CMOS based output stage. Koinuma utilizes bi-polar transistors for the transistor elements in the output stage. It is commonly known but Eng shows that a FET is an equivalent structure to a bi-polar design. See column 5, around line 63.

although the schematic diagrams show a bipolar transistor-based circuit, it is known by those skilled in the art that an equivalent FET-based circuit can be built.

Column 5, around line 63.

Therefore, because these two transistor structures were known as art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute the FET structure for the bipolar elements in Koinuma.

As to the CMOS input stage, Koinuma is silent on the exact construction of this stage. This is evidence that a conventional amplifier stage could be used. A specific structure that would be required other than the conventional is not recited and all Patents are presumed valid. 35 USC 282. Dudley in Figures 2 and 3 specifically recites that one conventional preamplifier stage is one that uses CMOS technology and thus that would inherently include FET structure.



Figures 2 and 3 of Dudley.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the generic amplifier of Koinuma with a CMOS based unit because as the Koinuma reference is silent on the exact structure of the preamplifier stage one of ordinary skill in the art would have been motivated to use any art-recognized equivalent preamplifier structure such as the CMOS based structure of Dudley.

In the combined structure made obvious above, the prior art is silent on mentioning the exact thicknesses of the input CMOS stage and the FET based output stage. However, it is commonly known that the lower operating voltage MOSFETs utilize a thinner oxide layer as compared to the higher operating voltage MOSFETs so that the thicker gate oxide layers can "reliably sustain higher voltages". Note column 1, around line 21 of Mandelman.

MOSFETs used in speed critical devices are customarily required to have properties such as short channels, low threshold voltages, and thin gate oxide layers. On the other hand, MOSFETs for use of interfacing with external circuitry are required to reliably sustain higher voltages so as to have thicker gate oxide layers and longer channels.

Column 1, around line 21 of Mandelman.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the oxide of the output stage thicker than the lower voltage input stage so that the higher output stage amplifier can "reliably sustain higher voltages" as taught by Mandelman.

The combination made obvious above is silent on the specific thickness of the two oxide layers, the thinner and thicker layers, with the thicknesses of 70 Angstroms and 140 Angstroms. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide such thicknesses, since it has been held that discovering an optimum value or workable range of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

As to the forming of the RF power amplifier arrangement made obvious above on or in a single integrated circuit, it is well known that to integrate a circuit results in a device that is more compact, more reliable than using a circuit based on discrete elements or components.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make for a more compact and more reliable structure in the device made obvious above by integrating that circuit on a single chip as is conventionally known in the art.

Applicant has added to the claims the language or language similar thereto:

> wherein the first gate oxide thickness is related to desired breakdown voltage levels of devices in the input stage circuitry and the second gate oxide thickness is related to desired breakdown voltage levels of devices in the output stage circuitry.

This recites a fact of nature or an inherent fact of all FET structures, namely that the gate oxide is related to the breakdown voltage and hence is related to the desired breakdown voltage. Clearly a FET with larger gate oxide thickness for oxides of the same material can withstand higher breakdown voltages. The examiner is not sure what structure applicant is implying by reciting this function. However, the

MPEP is clear that claims drawn to structure are to be distinguished from the prior art in terms of structure. (See MPEP 2114)

> >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >*In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997)

From MPEP 2114

The structure of the prior art inherently provides for this function. It is not clear what structure applicant may have actually meant for this phrase.

Response to Arguments

Applicant's arguments filed 12-15-2006 have been fully considered but they are not persuasive. Applicant states:

> The Examiner has taken the position that it would have been obvious to combine the teachings of these 5 references, and that such a combination makes the claims unpatentable

Applicant's point is not clearly stated, but it seems that applicant is implying that the number of references such as five (5) is evidence of non-obviousness? The examiner respectfully disagrees if this is the case. There may be many references that can make up a 35 USC 103 rejection. It appears to the examiner that the number of references is a showing of the thoroughness of the examiner's work in that it is a showing that the examiner finds the prior art should prior art exists for features of the claimed invention. The issue is not how many references are used but the issue is what the prior art as a whole teaches. The test for obviousness is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In the instant case the number of references is due to the fact that these references teach common engineering sense type things, like it is commonly known that a FET based circuit can be made from Bi-polars or that a higher operating voltage for a FET means that the gate oxide has to be thicker compared to a FET with a operating voltage that is lower than the "higher operating voltage". Other common engineering type things include that Class A, B, AB, C, D etc. can be used in a transceiver arrangement.

Applicant also states on page 8 of 10 of the remarks that:

There is no suggestion or motivation

in the 5 references to combine the teachings of the references as outlined in the Office Action.

The examiner respectfully disagrees. For example, the teaching of FET based circuits can be composed of Bi-polar based circuits, i.e. FETs and Bi-polars are equivalents is a motivation to replace Bi-polar with FETs and FETs with bi-polars. In Koinuma US 4,451,802 states what is not stated in many cascaded amplifier arrangements and that is the final amplifier structures have higher voltages than the earlier stages and Mandelman US 6,355,531 states what is not stated in these cascade amplifier arrangements is that the higher voltage structures have thicker gate oxides as compared to the FETs that are operated at a lower voltage than the "higher voltage structures".

Applicant states:
"As stated in the Specification:"

> "The RF amplifier of the present invention takes advantage of the availability of dual gate oxide devices by selectively choosing certain gate lengths for various components of the amplifier. For example, it has been discovered that for preprocessing circuitry or pre-driver circuitry, a high speed is desirable and breakdown voltage is not as important. Therefore these devices are designed using a thinner gate oxide. For output state devices, where a high breakdown voltage is more important, the devices are designed using a thicker gate oxide." (Specification, Page 28, lines 18-24).

Page 9 of 10 of applicant's remarks.

This seems to imply that the prior art does not teach the providing of the thicker oxide for the higher voltage transistors. The examiner respectfully disagrees for the Mandelman US 6,355,531 reference teaches substantially the same thing. Note column 1, around line 30.

> For example, MOSFETs used in speed critical devices are customarily required to have properties such as short channels, low threshold voltages, and thin gate oxide layers. On the other hand, MOSFETs for use of interfacing with external circuitry are required to reliably sustain higher voltages so as to have thicker gate oxide layers and longer channels

Column 1, around line 30 of Mendelman.

With lower voltage devices high speed is desirable, yet Mandelman says the same speed critical devices have low threshold voltages and thin gate oxide layers. Applicant states that he/she has discovered that for output devices "a higher breakdown voltage is more important", yet Mandelman says

the same for thicker gate oxides are required to "reliably sustain higher voltages", i.e. higher breakdown voltage is more important.

Applicant also states:

> This would tend to make a designer use the smallest gate oxide thickness available (since thin gate oxide devices are typically faster and more efficient). It may seem counter intuitive to use larger than available gate oxide thicknesses in an RF power amplifier. However, by following the teachings of the present application, a CMOS RF power amplifier can be designed with some devices utilizing the "less desirable" thicker devices. By carefully selecting the gate oxide thicknesses, a resulting design can have advantages over other devices (e.g., having certain devices with higher breakdown voltages).

The examiner does not exactly know what applicant is trying to say here for looking at the claims the claims states that the first gate oxide thickness is less than the second gate oxide thickness. The examiner does not see this in any of the independent claims and applicant has not pointed to specific claim language structure where the oxide used is "the less desirable thicker devices". The examiner has pointed out in the previous and present Office actions that not only is an (singular) optimum gate oxide thickness is obvious, but the selection of the whole workable range merely involves routine skill in the art and as this selection of thickness involves but routine skill, one of ordinary skill clearly would have found the selection of this range obvious. This workable range would include the less desirable thicker devices".

Applicant has added to the claims the language or language similar thereto:

> wherein the first gate oxide thickness is related to desired breakdown voltage levels of devices in the input stage circuitry and the second gate oxide thickness is related to desired breakdown voltage levels of devices in the output stage circuitry.

This recites a fact of nature or an inherent fact of all FET structures, namely that the gate oxide is related to the breakdown voltage and hence is related to the desired breakdown voltage. Clearly a FET with larger gate oxide thickness for oxides of the same material can withstand higher breakdown voltages.

The examiner is not sure what structure applicant is implying by reciting this function. However, the MPEP is clear that claims drawn to structure are to be distinguished from the prior art in terms of structure. (See MPEP 2114)

> >an< apparatus must be distinguished from the prior art in terms of structure rather than function. >*In re Schreiber*, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997)

From MPEP 2114

The structure of the prior art inherently provides for this function. It is not clear what structure applicant may have actually meant for this phrase.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker, can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
March 8, 2007

Michael B Shingleton
Primary Examiner
Group Art Unit 2815